METHOD FOR ISOLATING A HYBRID DEVICE IN AN IMAGE SENSOR

Technical Field ~~of the Invention~~

The present ~~invention~~ disclosure relates to an image sensor[[;]] and, more particularly, to an image sensor capable of ~~decreasing a~~ reducing the generation of dark current ~~generation through the use of~~ by using a hybrid device isolation process.

Description of Related Arts

Generally, an image sensor is a semiconductor device that ~~converts~~ changes an optical image into [[an]] electrical signals. ~~Particularly, a charge coupled~~ A charge-coupled device (CCD) is a device ~~wherein an~~ in which ~~individual metal-oxide-silicon (MOS)~~ capacitors ~~is closely allocated~~ are located close to each other[[,]]. ~~and an electrical~~ Electric charge carriers [[is]] are stored at the capacitors and ~~transferred to the MOS capacitor.~~ transmitted through the capacitors. A complementary metal-oxide semiconductor ~~device~~ (CMOS) image sensor is a device ~~that forms~~ constructed from as many MOS transistors as the ~~same~~ number of pixels. ~~and adopts a switching mode for sequentially detecting outputs with use of the MOS transistors~~ The CMOS image sensor uses a switching scheme to detect image outputs sequentially using the MOS

transistors by employing CMOS technology, and using a control circuit and a signal processing circuit as periphery circuits.

~~However, there~~ There are several problems [[of]] associated with using [[the]] a CCD due to its complex driving mode, high power dissipation, [[a]] complex fabrication process having ~~lots of~~ several steps for [[a]] the mask ~~process~~ processes, and [[a]] its difficulty in ~~one chip realization~~ being realized on one chip since [[the]] signal processing ~~circuit~~ circuitry cannot be constructed directly on [[a]] the CCD chip. Therefore, there has been ~~actively researched on the~~ active research related to a CMOS image sensor that uses sub-micron CMOS technology to overcome the ~~above~~ problems[[.]] noted above. [[The]] A CMOS image sensor obtains an image by forming a photodiode and a MOS transistor within a unit pixel and then uses a switching mode to sequentially ~~detecting~~ detect signals. ~~through a switching mode.~~ The use of [[the]] CMOS technology results in less power dissipation and ~~an enabled~~ enables the signal processing circuitry to be located on one chip. ~~one-chip process for the signal processing circuit.~~ Also, compared to the CCD process, ~~that~~ which requires approximately 30 to 40 masks, [[the]] a CMOS image sensor implemented with [[the]] CMOS technology is a simplified process that needs approximately 20 masks. ~~because of a simplified process. Hence,~~ Therefore, the CMOS[[,]] image sensor is currently highlighted as a next

generation image sensor.--

In a typical image sensor, dark ~~currents are~~ current is produced more easily, resulting in a decrease[[s]] in function and capability of the image sensor ~~storing~~ to store charges. ~~More~~ A more detailed explanation ~~on the~~ of dark current will be provided ~~in the following.~~ below.

Electrons[[,]] that move to a floating diffusion region from a photodiode[[,]] may produce dark current[[s]] even in [[an]] the absence of light. Particularly, [[the]] dark ~~currents are~~ current is caused by a dangling bond or various defects, such as a line defect, a point defect and so forth, that mainly exist in the edges of an activation region. Such dark current may cause severe problems in a ~~low illumination~~ low-illumination environment.

In a CMOS image sensor ~~to which a technology of providing~~ having a device line-width of about 0.35 μm or about 0.25 μm, as [[an]] the area of [[a]] the photodiode ~~region~~ decreases, a ratio of [[a]] the perimeter of the photodiode ~~region~~ with respect to the area of the photodiode ~~region~~ decreases as well.

~~The above feature is illustrated in FIG. 1.~~ Referring to FIG. 1, since three surfaces of the photodiode, except for [[a]] the surface in which a transfer transistor will be formed, are ~~touched to a~~ in contact with the field insulation layer, the photodiode is affected ~~in more extents~~ by the same defects generated at the edges of the

~~filed~~ field insulation layer as the photodiode area decreases due to micronization. ~~of a device. Herein, the~~ The perimeter of the photodiode is calculated ~~by taking~~ using only the three surfaces ~~touching to~~ in contact with the ~~filed~~ field insulation layer.

This effect of increasing dark current generation[[s]] with respect to an image signal is pronounced as [[a]] the minimum device line-width, e.g., about 0.25 μm or 0.18 μm, decreases. In other words, ~~such~~ a CMOS image sensor with an ultra fine line-width more easily causes [[the]] dark current.

Summary ~~of the Invention~~

~~It is, therefore, an object of the present invention to provide a~~ A method for isolating a hybrid device in an image sensor ~~through an improvement on a~~ by improving dark current characteristics even if [[an]] the area of [[a]] the photodiode region ~~decreases.~~ is reduced is disclosed.

In accordance with an aspect of the present ~~invention,~~ disclosure, ~~there is provided~~ a method for isolating a hybrid device in an image sensor includes: ~~including a photodiode, the method including the steps of:~~ forming sequentially a pad oxide layer and a pad nitride layer on a substrate and selectively removing a portion of the pad oxide layer and a first portion of the pad nitride layer to expose a surface of the substrate [[in]] on which a field

insulation layer will be formed; forming ~~the field insulation layer~~ a first ion-implantation region by performing a ~~channel stop~~ first ion-implantation process [[to]] on the exposed surface of the substrate ~~with use of~~ using the remaining pad nitride layer that exists after removal of the first portion of the pad nitride layer as a first mask; performing a thermal oxidation process to form the field insulation layer on the exposed surface of the substrate; removing a ~~partial~~ second portion of the pad nitride layer so that [[one]] a side of the remaining pad nitride layer that exists after removal of the second portion of the pad nitride layer is spaced ~~out with a predetermined distance from an edge of the field insulation layer;~~ apart from an edge of the field insulation layer by a distance; and forming a second ion-implantation region by performing ~~an additional~~ a second ion-implantation process ~~onto~~ on ~~the exposed substrate surface and~~ the field insulation layer [[by]] using the remaining pad nitride layer that exists after removal of the second portion of the pad nitride layer as a second mask.

Brief Description of the Drawing(s)

The above ~~and other objects and features of the present invention~~ will become apparent from the following description of ~~the preferred~~ embodiments ~~given~~ taken in conjunction with the accompanying drawings, in which:

Fig. 1 is an exemplary diagram showing a ratio of a photodiode perimeter with respect to a photodiode area in a typical image sensor;

FIGS. 2A to 2D are cross-sectional views showing a hybrid device isolation ~~process~~ region in an image sensor in accordance with ~~a preferred~~ one embodiment; ~~of the present invention;~~

FIG. 3 is a cross-sectional view showing a device isolation ~~process with~~ region having a trench structure in accordance [[with-another]] with another ~~preferred~~ embodiment; ~~of the present invention;~~

FIG. 4A is a plane view showing a layout of a photodiode and a transfer transistor in a unit pixel of a complementary metal-oxide semiconductor (CMOS) image sensor in accordance with yet another ~~preferred~~ embodiment; ~~of the present invention;~~ and

FIG. 4B is a cross-sectional view with respect to a line A-A' of FIG. 4A illustrating the photodiode and the transfer transistor in the unit pixel of the CMOS image sensor. ~~formed in accordance with the above preferred embodiment of the present invention~~.

Detailed Description ~~of the Invention~~

~~Figs. 2A to 2D are cross-sectional views showing a device isolation process in an image sensor in accordance with a preferred embodiment of the present invention.~~

Referring to FIG. 2A, a pad oxide layer 11, a pad nitride layer 12 and a photosensitive layer 13, which will be used as a device isolation mask in subsequent processes, are sequentially formed on a substrate 10. Then, a device isolation mask process is performed [[to]] on a region of the substrate 10 where a field insulation layer will be formed. ~~In the present invention, the~~ The substrate 10 can use a stack structure ~~wherein~~ in which an epitaxial layer with a low concentration is deposited on a silicon layer with a high concentration.

The ~~reason for using the~~ lowly concentrated epitaxial layer is used because it is possible to improve device properties by increasing [[a]] the depth of [[a]] the depletion layer of [[a]] the photodiode, [[and]] as well as to prevent ~~a cross-talk phenomenon~~ cross talk between unit pixels in a substrate with a high concentration.

Referring to FIG. 2B, the pad nitride layer 12 and the pad oxide layer 11 are etched ~~with use of~~ using the device isolation mask 13 ~~so as~~ to expose a surface of the substrate 10 [[in]] on which the field insulation layer will be formed. The device isolation mask 13 is removed ~~thereafter.~~ after the pad nitride layer 12 and the pad oxide layer 11 have been etched.

Next, a channel stop ~~ion implantation~~ ion-implantation process is performed to the surface of the substrate 10 by using the ~~exposed~~ etched pad nitride layer 12 as an ion-implantation mask ~~so as~~ to form a channel stop

ion-implantation region 100. For the channel stop ion-implantation[[,]] process, the [[an]] ion-implantation concentration of boron is about $3.0\text{x}10^{13}$ cm^{-3} and the ion-implantation energy [[are]] is about ~~$3.0\text{x}10^{13}cm^{-3}$ and about~~ 30 keV[[,]]. ~~respectively.~~ The above channel stop ion-implantation process is ~~proceeded~~ carried out without ~~giving~~ specifying a tilt angle and a ~~ration.~~ rotation angle.

With reference to FIG. 2C, ~~the surface of the substrate 10 completed with~~ after the channel stop ion-implantation process is completed, ~~is then proceeded with~~ a thermal oxidation process is performed ~~so as~~ to ~~grow~~ form the field insulation layer, ~~particularly,~~ e.g., a field oxide layer (Fox)[[.]] on the surface of the exposed substrate 10. ~~On the pad nitride layer 12, a~~ A photosensitive pattern 14 is subsequently formed on the pad nitride layer 12 to etch the pad nitride layer 12 ~~with~~ so that a side of the pad nitride layer 12 is spaced apart ~~a predetermined distance X~~ from an edge of the Fox[[.]] by a predetermined distance X. ~~At this time, the~~ The predetermined distance X ~~preferably~~ ranges from about 0.5 μm to about 1.0 μm.

With reference to FIG. 2D, the pad nitride layer 12 is etched ~~with~~ so that a side of the pad nitride layer 12 is spaced apart ~~the predetermined distance X~~ from the edge of the Fox by the predetermined distance X by using the photosensitive pattern 14 as an etch mask. Subsequently, a boron ion-implantation process is performed on the Fox by

using the etched pad nitride layer 12 as an ion-implantation mask.

~~At this time, the~~ The boron ion-implantation process can be carried out [[at]] under the same conditions [[of]] as the channel stop ion-implantation process. [[or]] Alternatively, the boron ion-implantation process can be carried out [[by]] using a boron concentration ranging from about 4.0 x 10^{13} cm^{-3} to about 5.0 x 10^{13} cm^{-3}. Such an optimal dosing concentration is determined after receiving [[a]] feedback information about [[a]] dark current characteristics.

Referring to FIG. 2D, ~~denoted numerical symbols, 1 and 2, represent~~ the numerical symbol "1" enclosed in a circle represents the channel stop ion-implantation region 100 formed by the channel stop ion-implantation process, and the numerical symbol "2" enclosed in a circle represents a boron ion-implantation region 50 ~~additionally~~ formed ~~through~~ by the boron ~~ion implantation~~ ion-implantation process[[,]]. ~~respectively.~~ ~~Also, as shown, the~~ The photosensitive pattern 14 is removed after ~~completing~~ the ~~additional~~ boron ion-implantation process[[.]] is performed.

In accordance with ~~the preferred~~ one embodiment, ~~of the present invention,~~ the boron ion-implantation region 50 ~~screens~~ encompasses the edges of the Fox, thereby improving [[the]] dark current characteristics. ~~That is,~~ In other words, electrons generated at the edges of the Fox ~~are disappeared through an~~ disappear by electron-hole ~~electron~~

~~hole~~ pair recombination, ~~phenomenon~~ which occurs at the boron ion-implantation region 50.

FIG. 3 is a ~~plane~~ cross-sectional view showing a device isolation ~~process with~~ region having a trench structure in accordance with another ~~preferred~~ embodiment. ~~of the present invention.~~ As with FIG. 2D, a [[A]] channel stop ion-implantation region [[1]] is represented by the numerical symbol "1" enclosed in a circle, and a boron ion-implantation region [[2]] is represented by the numerical symbol "2" enclosed in a circle ~~are illustrated~~ in FIG. 3.

~~The following is a detailed description on a preferred embodiment of a process for forming a device isolation region having a trench structure.~~

Referring to FIG. 3, a process for forming a device isolation region having a trench structure is described. A buffer oxide layer (not shown) and a pad nitride layer (not shown) are sequentially deposited on a substrate 20. ~~Then, a~~ A device isolation mask is then used to selectively etch the buffer oxide layer and the pad nitride layer so that a region[[,]] in which a trench will be formed[[,]] is exposed. Afterwards, the trench is formed [[on]] in the substrate 20 ~~with use of~~ by an etch process using the pad nitride layer as an etch mask. ~~Subsequent to~~ After the trench formation, an oxide layer is formed in an inner wall of the trench ~~in order~~ to compensate for ~~damages of~~ damage to the inner wall of the trench that ~~occurs when proceeding~~ occurred during the etch process. ~~for forming the trench.~~

Next, a channel stop ion-implantation process is performed to form the channel stop ion-implantation region, [[1]] which is represented by the numerical symbol "1" enclosed in a circle in FIG. 3, and ~~bury~~ an insulation material 21 is deposited in the trench. ~~with an insulation material 21.~~ The insulation material 21 in the trench is planarized ~~through~~ by a chemical mechanical polishing (CMP) process, and ~~then,~~ a predetermined portion of the pad nitride layer is then etched ~~in such a manner~~ so that one side of the pad nitride layer is spaced ~~out with a predetermined distance~~ apart from an edge of the insulation material 21[[.]] by a predetermined distance.

After the ~~above~~ etching process, a boron ion-implantation process is ~~additionally~~ performed by using the pad nitride layer as an ion-implantation mask ~~so as~~ to form a boron ion-implantation region, [[2]] which is represented by the numerical symbol "2" enclosed in a circle in FIG. 3. ~~on the exposed substrate 20 and the insulation material 21.~~ The pad nitride layer is removed thereafter, ~~whereby the~~ and a device isolation region ~~with~~ having a shallow trench isolation structure is ~~completely~~ formed.

In addition to a typical device isolation process ~~with~~ using a local oxidation of silicon (LOCOS) structure, the present ~~invention~~ disclosure can [[be]] also be applied to a device isolation process ~~with~~ using a trench structure or a poly buffered locos (PBL) process.

FIG. 4A is a plane view showing a layout of a

photodiode and a transfer transistor in a unit pixel of a complementary metal-oxide semiconductor (CMOS) image sensor ~~formed~~ in accordance with another ~~preferred~~ embodiment. ~~of the present invention. Especially, a~~ A boron doping profile is ~~formed by being~~ spaced out ~~with~~ a predetermined distance ~~in a photodiode region contacting to~~ from a Fox (not shown). A boron ion-implantation region ~~additionally ion-implanted encompasses~~ encompasses the edges of the Fox[[,]] and, therefore, ~~this fact~~ ~~provides an effect of decreasing~~ reduces dark current[[s]] even if an n-type ion-implantation region ~~for a~~ of the photodiode is not ~~decreased~~ reduced to a size to fit within [[a]] the dotted boundary[[.]] shown in FIG. 4A. It is also possible to prevent a ~~decrease~~ reduction of saturation current[[s]] since it is not necessarily required that the n-type ion-implantation region [[for]] of the photodiode ~~is not necessarily required to be decreased for improving the~~ be reduced to improve dark current characteristics.

FIG. 4B is a cross-sectional view showing the photodiode region and the transfer transistor ~~from a viewpoint of~~ with respect to the [[A-A']] line A-A' shown in FIG. 4A.

The structure ~~shown~~ illustrated in FIG. 4B includes a Fox layer 31 formed on a substrate 30, a channel stop ion-implantation region 32A formed on [[a]] the bottom of the Fox layer 31, a boron ion-implantation region 32B ~~extended with~~ extending a predetermined distance from an edge of the

Fox layer 31, an n-type ion-implantation region 34 ~~for a~~ of the photodiode formed within the substrate 30 and ~~contacted to~~ in contact with one side of the Fox layer 31, a spacer 35 formed on lateral sides of a gate electrode 33 of the transfer transistor, a p-type ion-implantation region 36 for [[a]] the photodiode formed in between [[a]] the surface of the substrate 30 and the n-type ion-implantation region 34 for the photodiode, and a floating diffusion region 37 formed on the other side of the p-type ion-implantation region 36 for the photodiode and the transfer transistor. ~~Herein, one~~ One side of the p-type ~~ion implantation~~ ion-implantation region 36 for the photodiode is ~~contacted to~~ in contact with the spacer 35 and the other side of the p-type ion-implantation region 36 of the photodiode is in contact with ~~is contacted to~~ the boron ion-implantation region 32B.

As ~~shown,~~ illustrated in FIG. 4B, the boron ion-implantation region 32B ~~extended with the~~ extends a predetermined distance from an edge of the Fox layer 31 and encompasses ~~screens~~ the edge of the Fox layer 31[[,]]. ~~and this~~ This encompassing action suppresses dark current[[s]] generated ~~from~~ at the edge of the Fox layer.

~~In case of implementing this inventive method to an image sensor, it~~ It is possible to improve [[the]] dark current characteristics even in a micronized structure ~~through the use of~~ by using this hybrid device isolation technique. Also, [[a]] it is not necessarily required that

the photodiode ~~region is not necessarily required to~~ be ~~decreased~~ reduced to ~~make an improvement on the~~ improve dark current characteristics. Therefore, it is possible to obtain a clearer and well-defined image since saturation currents can [[be]] also be ~~decreased.~~ reduced.

While the present ~~invention~~ disclosure has been described with respect to certain ~~preferred~~ embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the ~~invention~~ disclosure as defined in the following claims.

Abstract of the Disclosure

The present ~~invention~~ disclosure relates to a method for fabricating an image sensor capable of improving [[a]] dark current characteristics. The method includes: ~~the steps of:~~ forming sequentially a pad oxide layer and a pad nitride layer on a substrate and selectively removing a portion of the pad oxide layer and a first portion of the pad nitride layer to expose a surface of the substrate [[in]] on which a field insulation layer will be formed; forming ~~the field insulation layer~~ a first ion-implantation region by performing a first ~~channel stop~~ ion-implantation process [[to]] on the exposed surface of the substrate ~~with use of~~ using the remaining pad nitride layer that exists after removal of the first portion of the pad nitride layer as a first mask; performing a thermal oxidation process to form the field insulation layer on the exposed surface of the substrate; removing a ~~partial~~ second portion of the pad nitride layer so that [[one]] a side of the remaining pad nitride layer that exists after removal of the second portion of the pad nitride layer is spaced ~~out with a predetermined distance from an edge of the field insulation layer;~~ apart from an edge of the field insulation layer by a distance; and forming a second ion-implantation region by performing ~~an additional~~ a second ion-implantation process ~~onto~~ on ~~the exposed substrate surface and~~ the field insulation layer [[by]] using the remaining pad nitride layer that exists after removal of the second portion of

the pad nitride layer as a second mask.